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Software-Compiled System Design

Early Models in Silicon with SystemC synthesis

Agility Compiler summary

- C-based design & synthesis for SystemC
- Pure, standard compliant SystemC/ C++
- Most widely used C-synthesis technology
- Structural SystemC output for design verification
- Deterministic and predictable synthesis
- Automatically generates IEEE RTL VHDL & Verilog
- Automatically generates FPGA netlists
- Supports multiple clock domains
- Supports synthesis for multiple blocks

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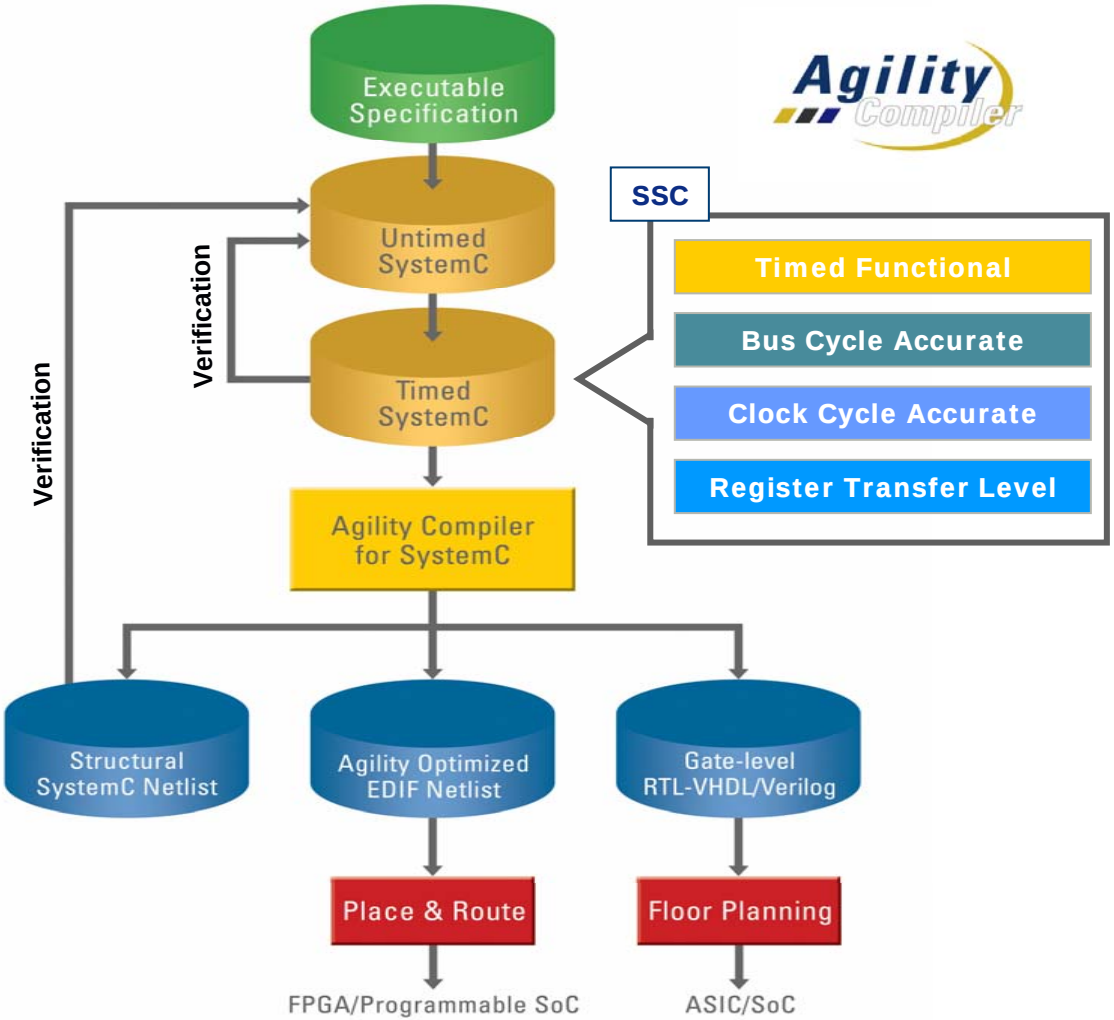
Agility Compiler flow chart



- **Verification centric implementation**
- **Early models to rapid prototype in high density FPGA**
- **Accurate performance metrics from silicon earlier**
- **Yields timing information earlier**
- **Predictable synthesis**
- **RTL output feeds ASIC/ SoC implementation tools & flows**
- **Silicon independent**

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Cut to live demo…

Agility Compiler

Agility Compiler overview features

- Built on the most widely used C-synthesis technology
  - Supports the OSCI SystemC synthesizable subset
  - Pure SystemC with no proprietary descriptions
- Extended synthesis support
  - Features over and above the synthesizable subset include:
  - `sc_fifo`
  - Compile time C++ math.h library support
  - Compile time support for float and double types
  - Single Port RAM/ Dual Port RAM
- Automatic generation of RT Level VHDL and Verilog
  - VHDL IEEE 1076.6 – 1999
  - Verilog IEEE 1364 – 2001
  - Design Compiler optimization Q3, 05
- Automatic generation of Actel, Altera, Xilinx EDIF netlists
  - Inc. Cyclone II, Stratix II, Spartan3 & Virtex4

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Agility Compiler overview features

- Automatic generation of RTL Structural SystemC output
  - Verify designs against the original testbench
- Powerful synthesis optimizations
  - Examples include: re-timing, fine grained logic sharing, automatic tree balancing
- True ‘system’ design capabilities
  - Synthesize a complete hardware system (does not restrict the designer to single blocks)
  - Supports any number of hierarchical modules with any number of processes
- Multiple clock domain support
  - Easy to design, refine and synthesize multiple clock domain designs

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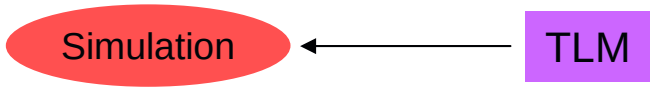
Functional Verification

- **Start from SystemC TLM and testbench**



- **Refine module for synthesis**
- **Synthesize module to EDIF/ RTL or SystemC**
- **Verify SystemC with original testbench and/ or RTL output**
- **Implementation**

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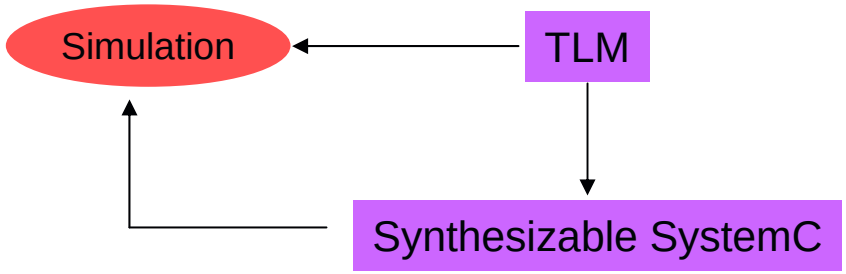
Refinement

- Start from SystemC TLM and testbench
- Refine module for synthesis
- Synthesize module to EDIF/ RTL or SystemC
- Verify SystemC with original testbench and/ or RTL output
- Implementation



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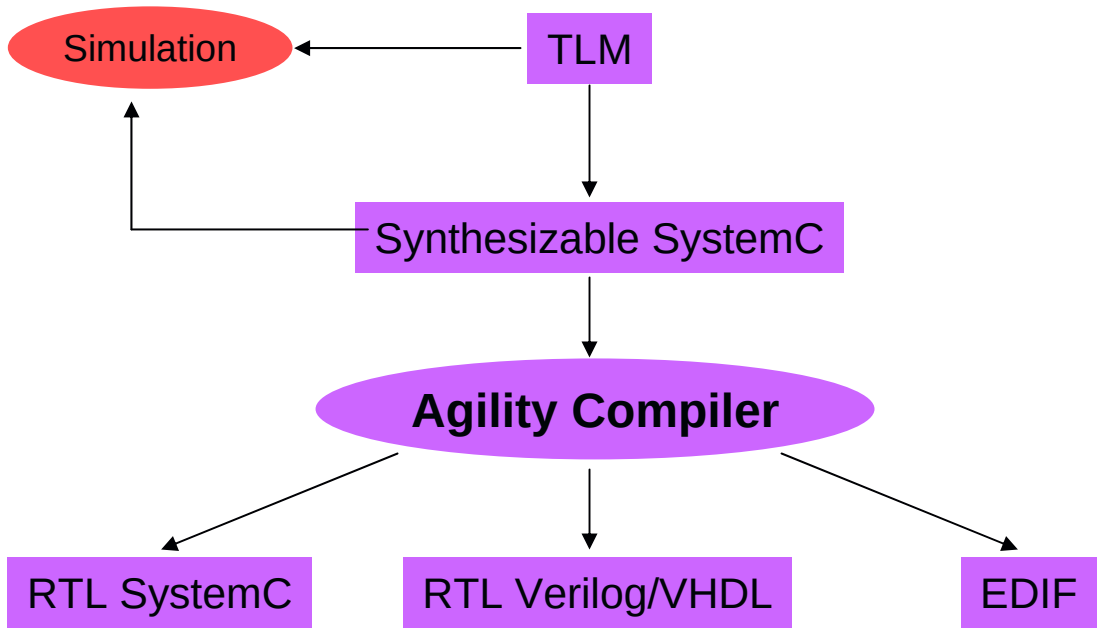
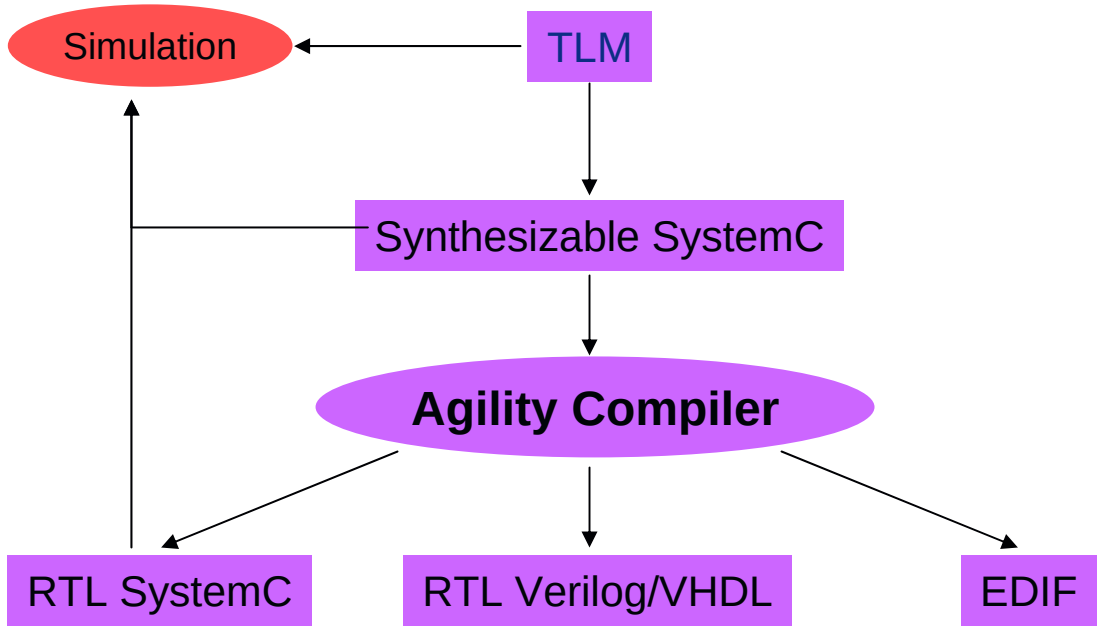
Synthesis

- **Start from SystemC TLM and testbench**
- **Refine module for synthesis**
- **Synthesize module to EDIF/ RTL or SystemC**
- **Verify SystemC with original testbench and/ or RTL output**
- **Implementation**



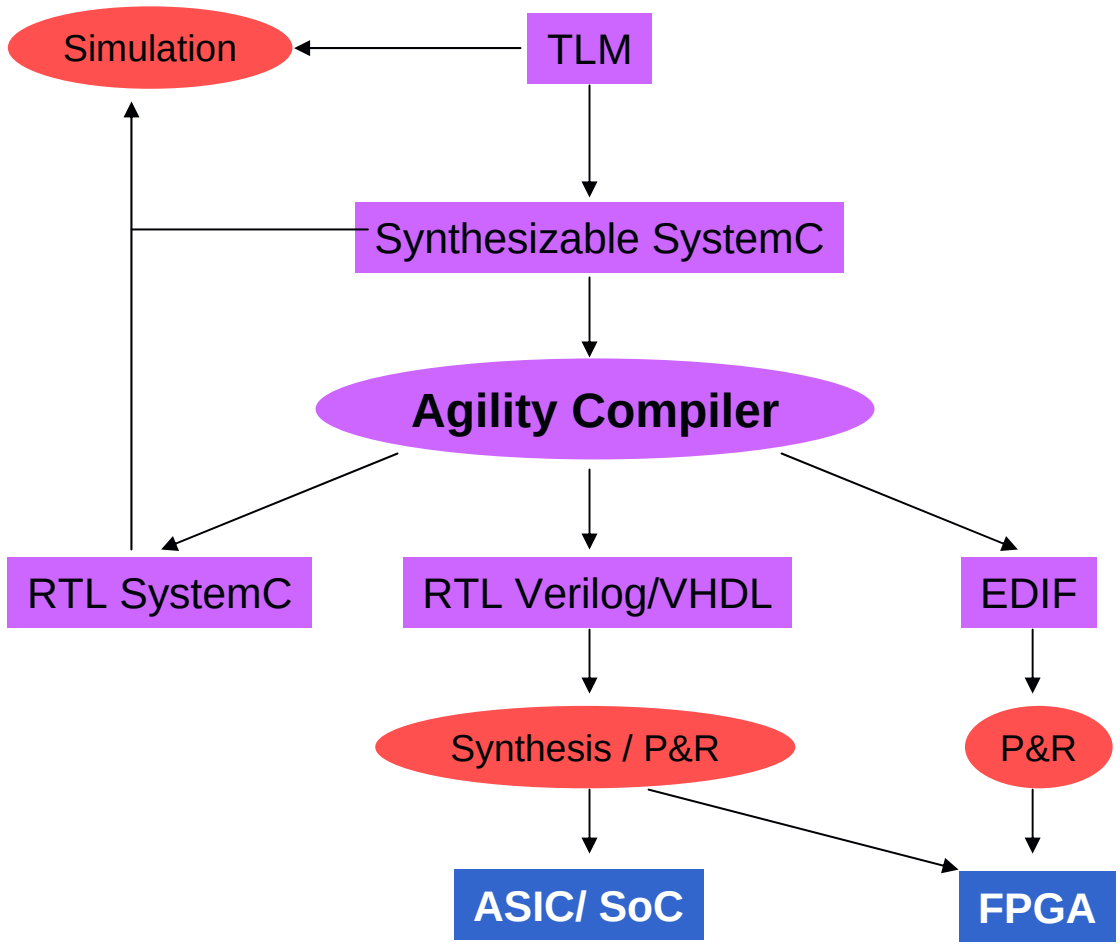
Post synthesis verification

- **Start from SystemC TLM and testbench**
- **Refine module for synthesis**
- **Synthesize module to EDIF/ RTL or SystemC**
- **Verify SystemC with original testbench and/ or RTL output**
- **Implementation**



Implementation

- Start from SystemC TLM and testbench
- Refine module for synthesis
- Synthesize module to EDIF/ RTL or SystemC
- Verify SystemC with original testbench and/ or RTL output
- **Implementation**



P&R: Place and Route

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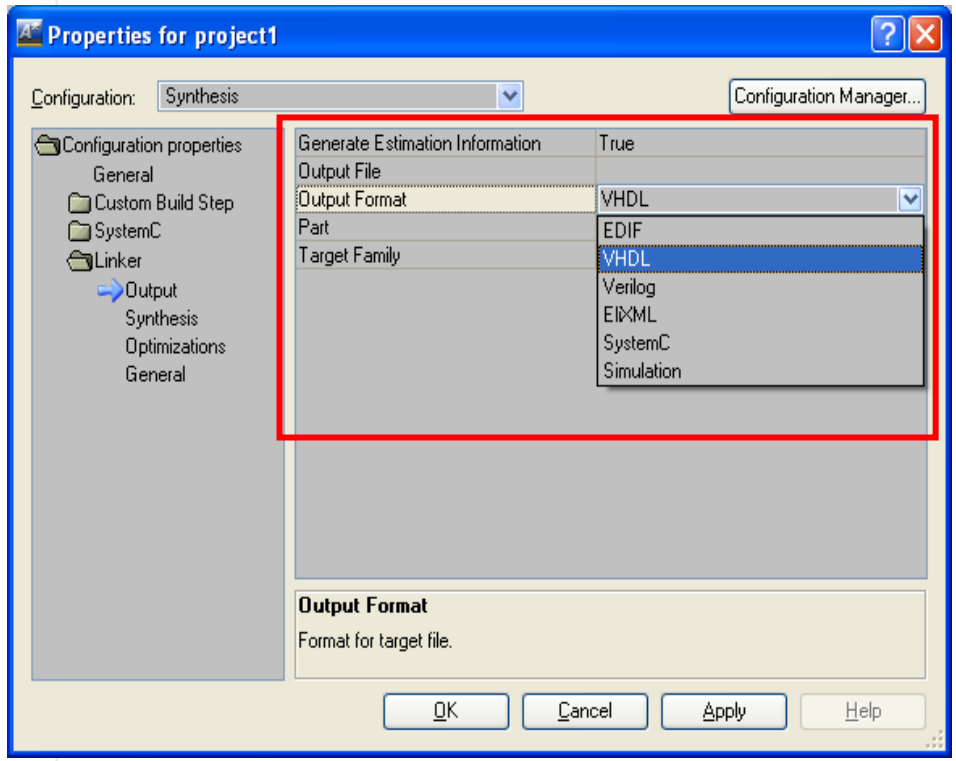
Synthesis output formats

- **Automatic generation of RT Level VHDL and Verilog**
  - **VHDL IEEE 1076.6 – 1999**
  - **Verilog IEEE 1364 – 2001**
- **Automatic generation of Actel, Altera, Xilinx EDIF netlists**
  - **Inc. Cyclone II, Stratix II, Spartan3 & Virtex4**
- **Automatic generation of RTL Structural SystemC output**
  - **Verify designs against the original testbench**



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Design analysis and reporting

Area & delay estimation

Logic used for each line of code

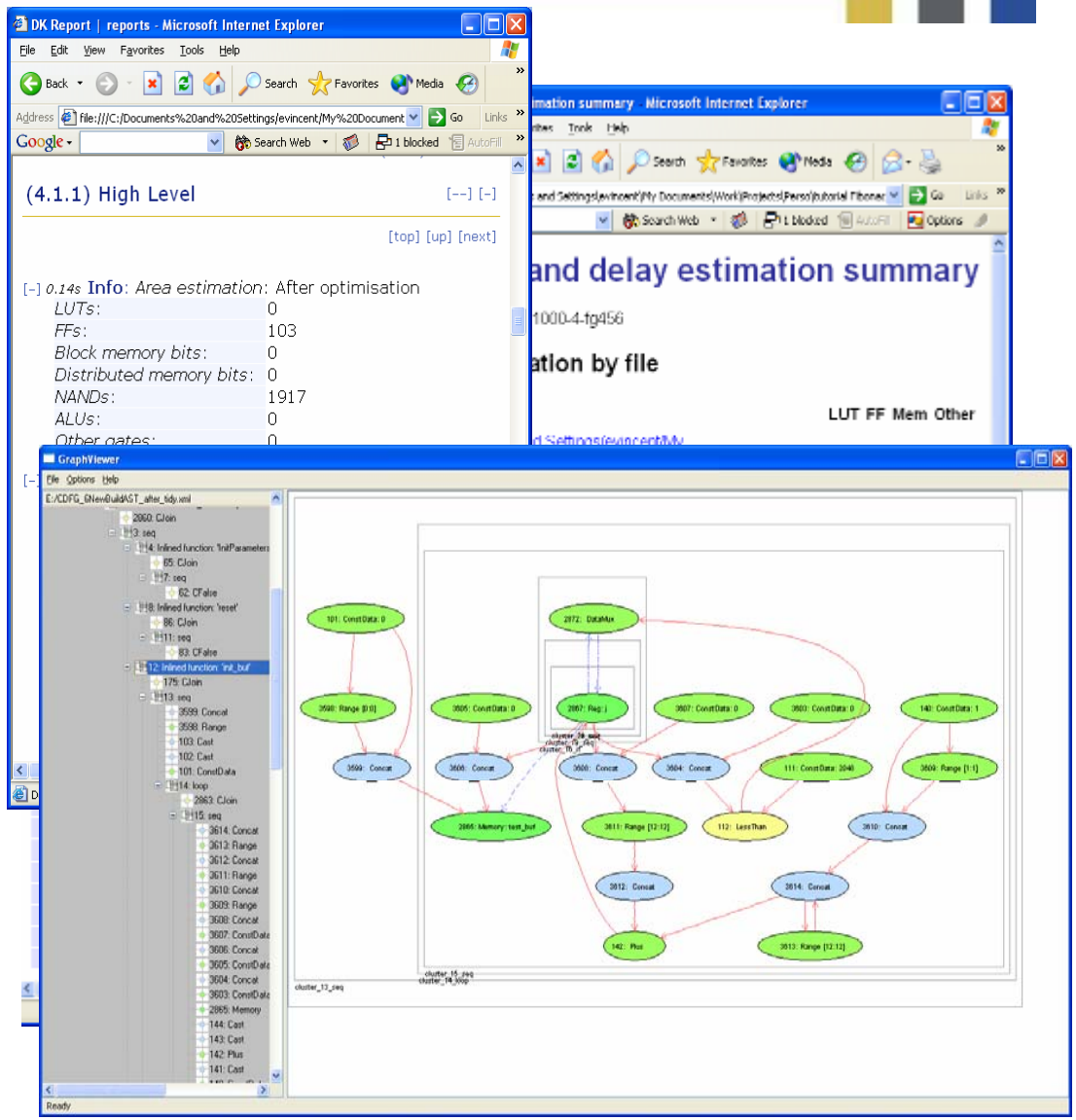
Critical path analysis

Synthesis reports & logic block analysis

Supporting architectural exploration and design optimization

Control & dataflow analysis

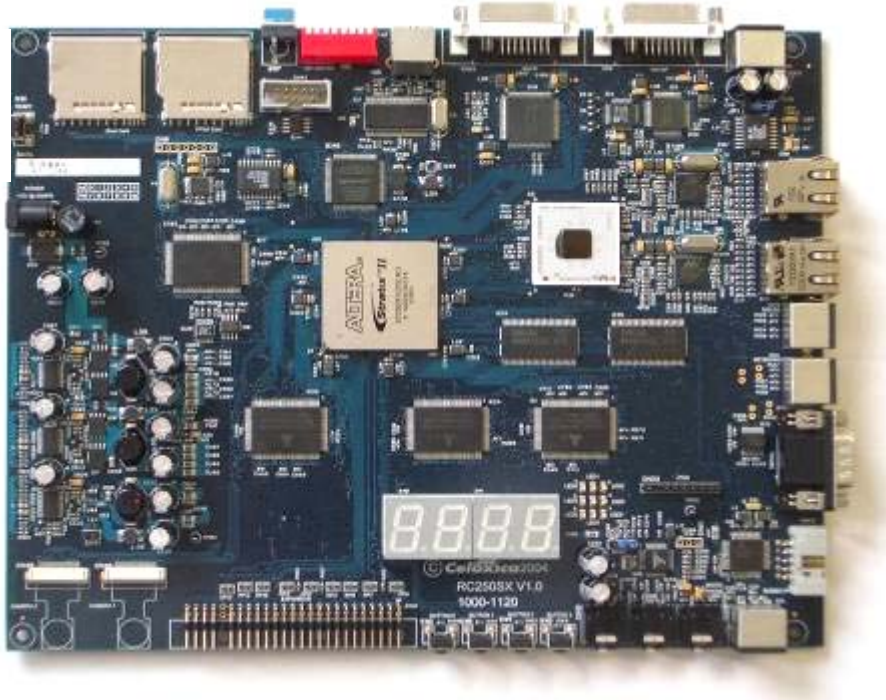
Graphical tool for exploring the control and data flow graph



Agility Compiler evaluation kit

- **Software, libraries & programmable SoC hardware for SystemC modeling, verification & synthesis**
- **Direct synthesis to FPGA device**

RC250 series



Prototyping & development of high performance/ high throughput SystemC applications

Altera Stratix II FPGA

1x EP2S90 (9 million gate device)

Memory

4 banks of 1Mx36 ZBT

64 MBytes SDRAM

USB 2.0 connection

Fast data transfers to host applications (e.g. *"hardware-in-the-loop"*)

Supports new "legacy-free" PCs and laptops

Dual SD card for Flash & SDIO

DVI and analogue video in & out

Audio in & out

Dual Gigabit Ethernet

Dual 2MPixel cameras

Expansion via ATA compatible header

8 1/2" flat panel screen

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Conclusions

- Built on the worlds most widely used C-synthesis technology
- Pure SystemC/ C++
- SystemC synthesis solution:
  - Automatically generate IEEE RTL VHDL & Verilog
  - Automatically generate FPGA netlists
  - Automatically generates Structural SystemC
  - Support multiple clock domains
  - Support synthesis for multiple blocks