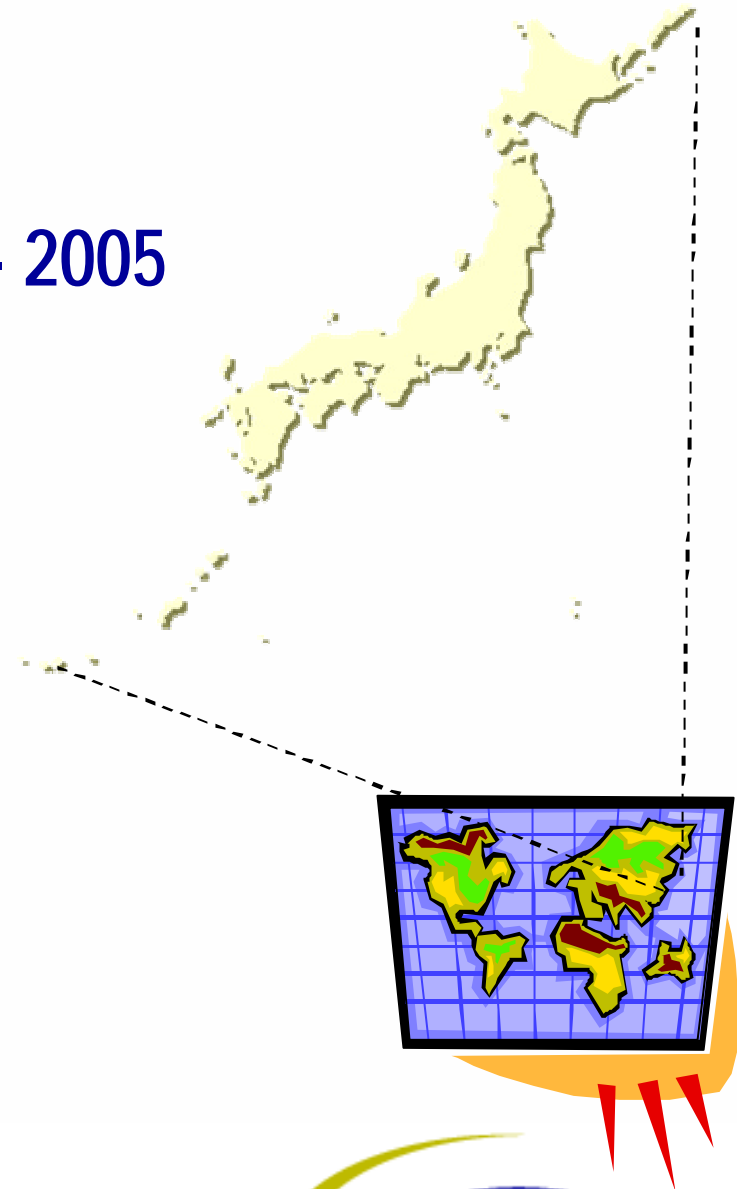# SystemC in Japan

March 8th, 2005

Masamichi Kawarabayashi

Japan Promotion Group, OSCI

# Outline

- **SystemC promotion in Japan**
- **SystemC users survey in 2003 - 2005**
  - Application area
  - Current language
  - SystemC usage
  - Key technology
- **Design examples**
  - Fujitsu Network Technologies
  - NEC Electronics
  - Toshiba
- **Summary**

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# SystemC promotion in Japan

- Seminar
  - 5 official seminars(2001, 2002, 2003, 2004, 2005) at EDS Fair
  - SystemC Design Workshop, Aug 2003, Oct 2004, CQ Publishing
  - SystemC tutorial and OSCI booth, Nov 2003, 2004, @Embedded Technology Conference
  - and more
- Education: Training companies
  - Ishizue, HD Lab, Hitachi-IT, Cadence
- Publication: books, magazines
  - System Design with SystemC, Japanese translation (Maruzen Publishing)
  - VLSI design with C/C++ - JPEG codec design with SystemC – (Kyoritsu Publishing)
  - Series articles in Design Wave Magazine

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# SystemC survey summary

- Compared the survey results in 2003 through 2005 at Japan SystemC Users Forum.

| Year | 2005 | 2004 | 2003 |
|------|------|------|------|
| # of participants | * 247 | 327 | 420 |
| # of surveys | 195 | 261 | 320 |

*: conference room was full.

- "investigating" in 2003 to "utilizing" in 2004-2005

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# 2. What is your application?



multiple choice
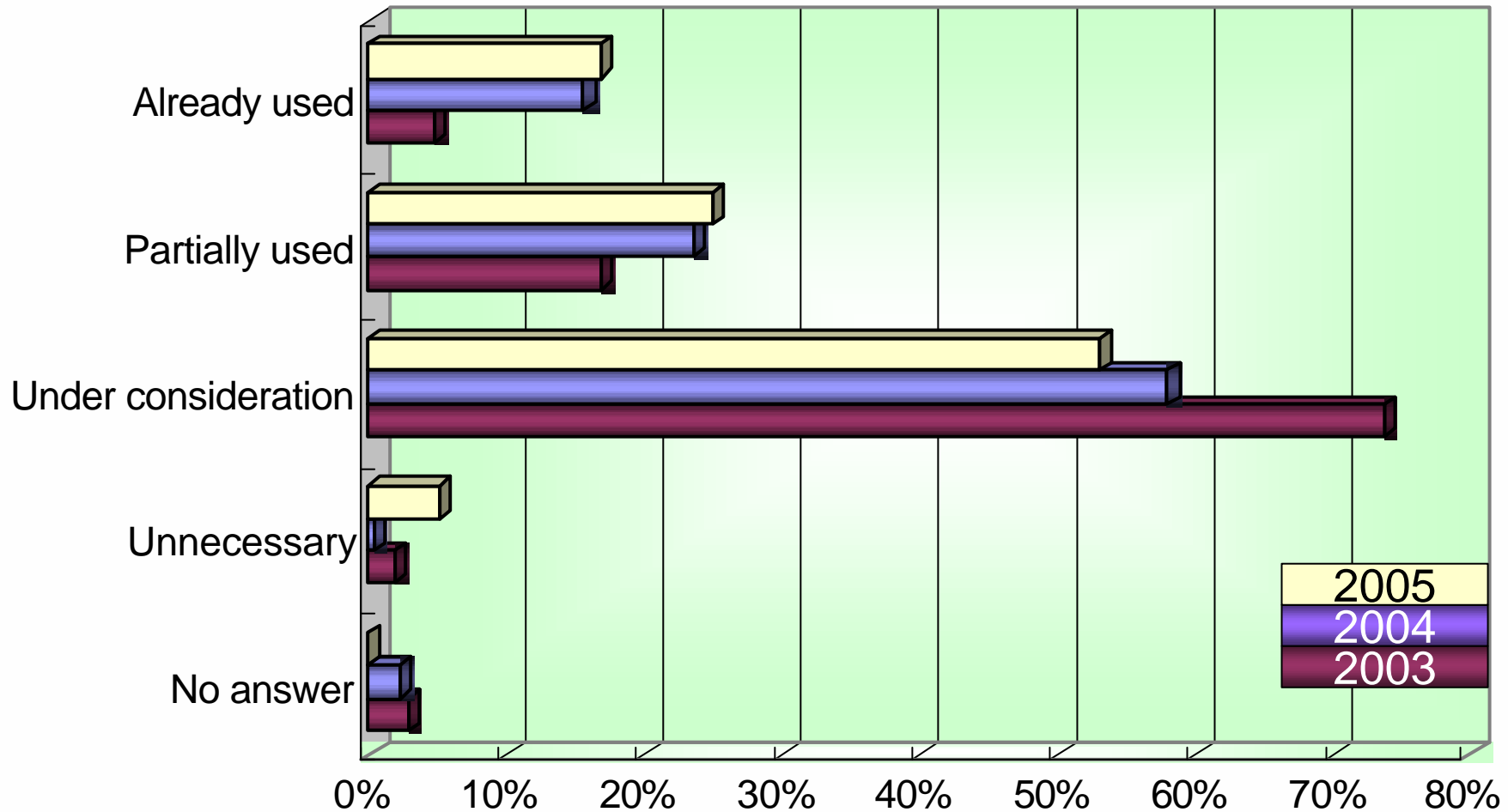
**"SystemC in Japan" @11th European SystemC Users Group, 2005**
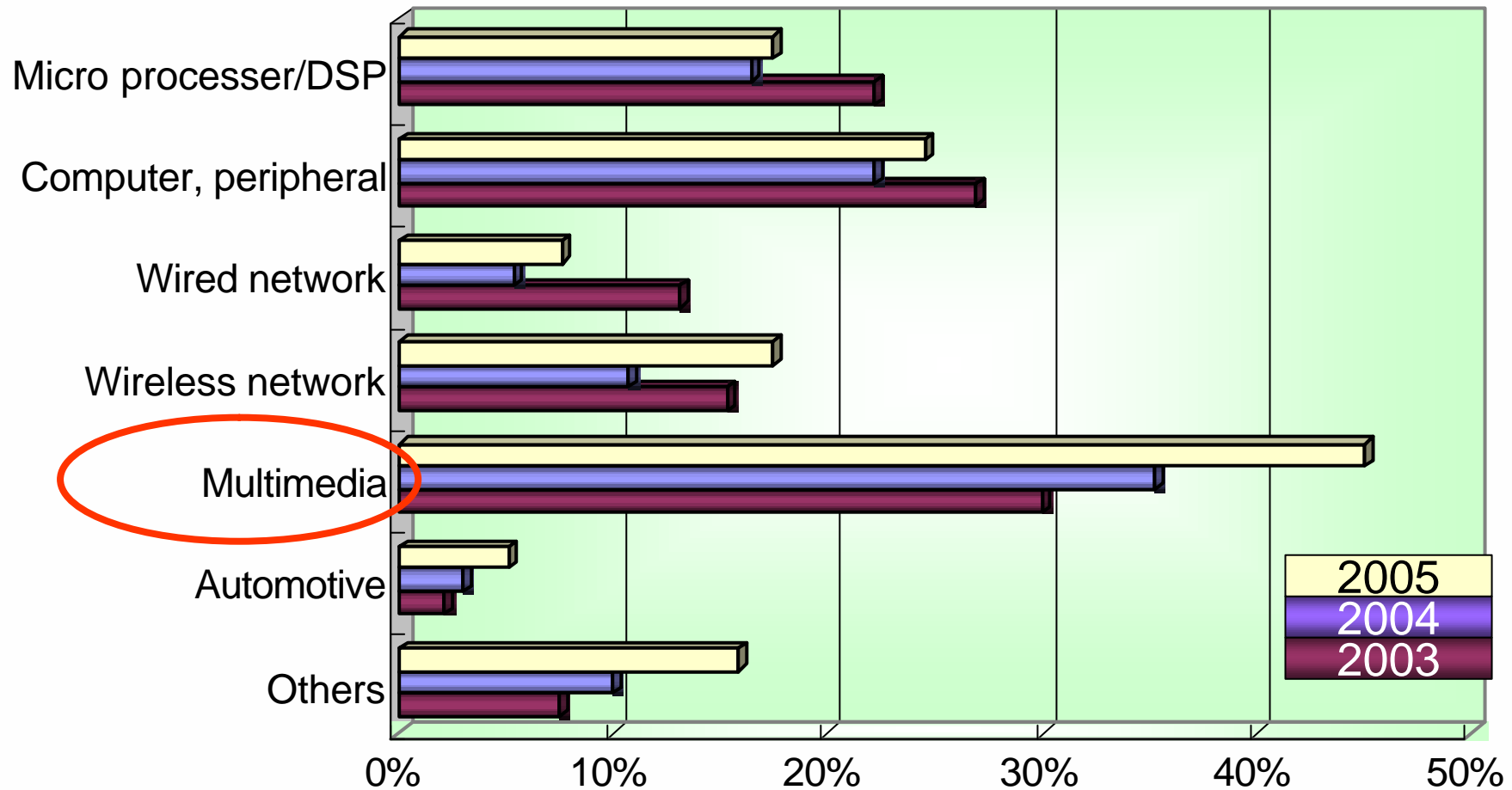
# 3. What language do you use for design, modeling and/or verification?
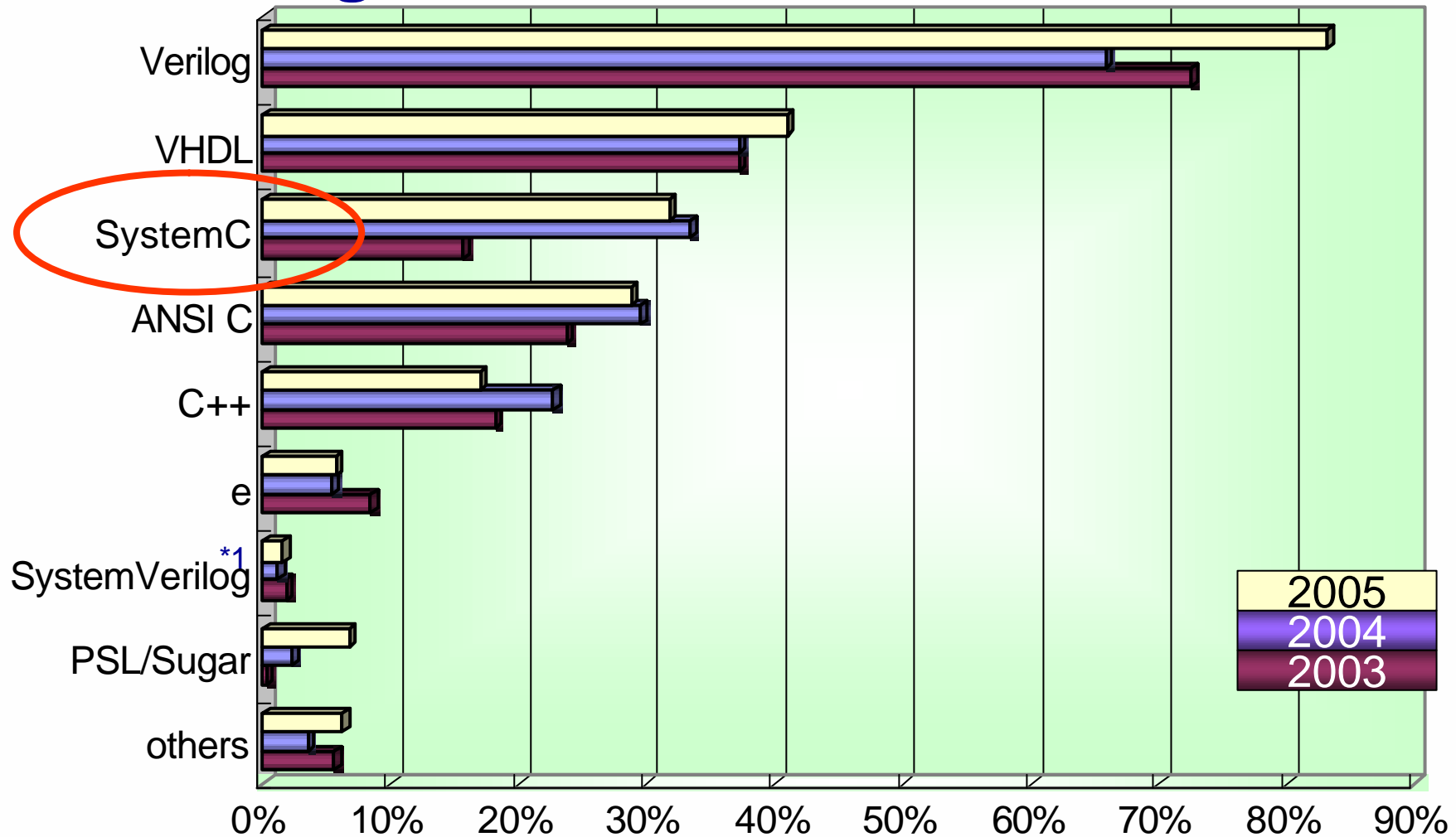


*1: Asked "OpenVERA" in 2003, "SystemVerilog" in 2004-5.  multiple choice

**"SystemC in Japan" @11th European SystemC Users Group, 2005**

# 5. Do you use SystemC for design, modeling, and/or verification?

# 9. What kind of improvements are necessary to encourage more utilization of SystemC?



multiple choice

**"SystemC in Japan" @11th European SystemC Users Group, 2005**
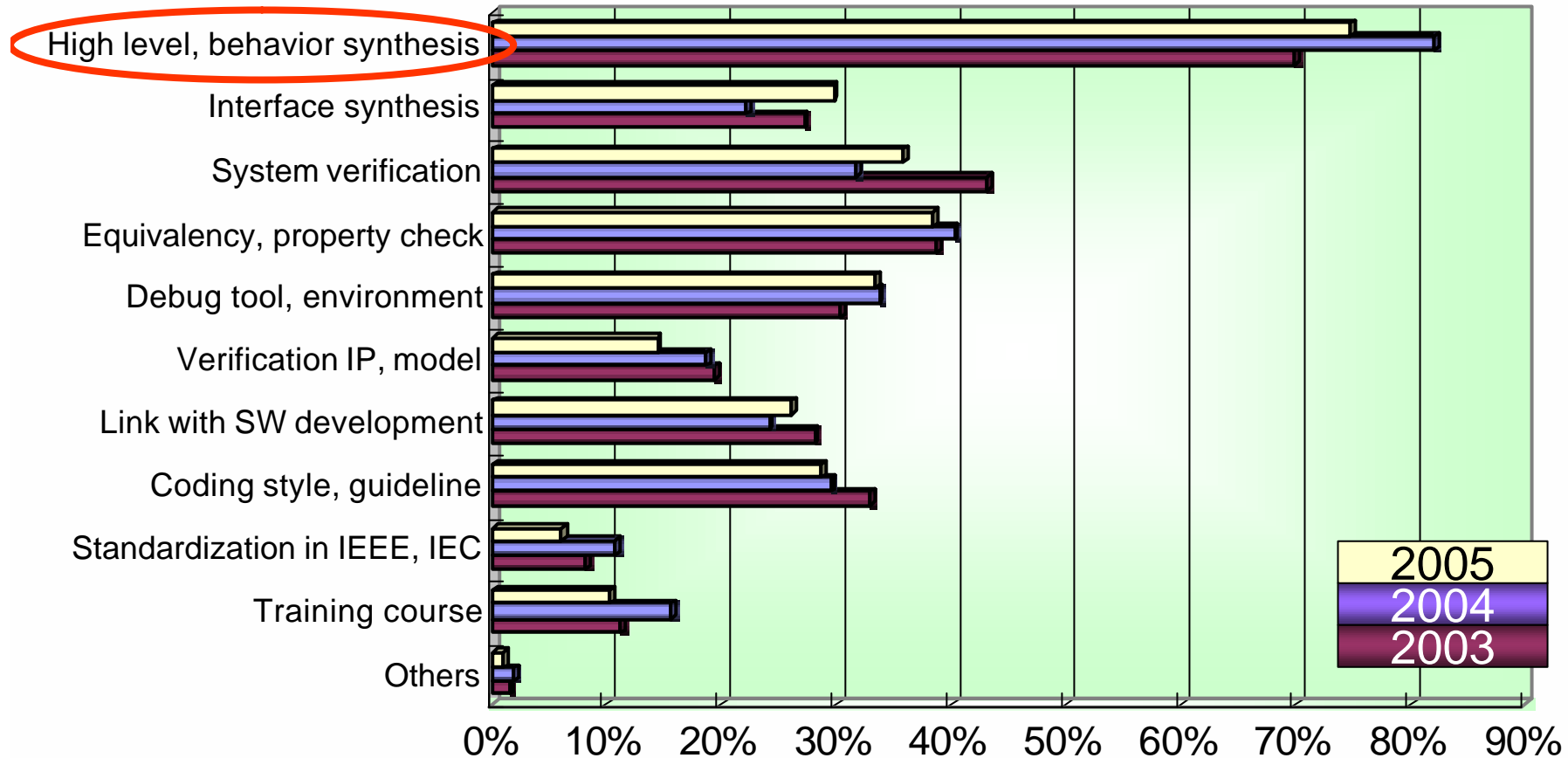
# Fujitsu Network Technologies : Speech enhancement algorithm hardware

*Collaboration among industry, government and academia*

Aging of population causes an increase in the number of hearing impaired persons,and requires the hearing aid technologies. This project aims to develop the hearing aid LSI for audio equipment.
Using SystemC, the implementation time from algorithm researched in C description to hardware can be reduced.
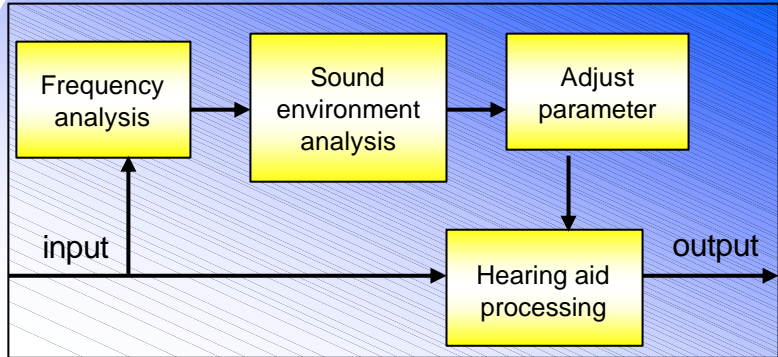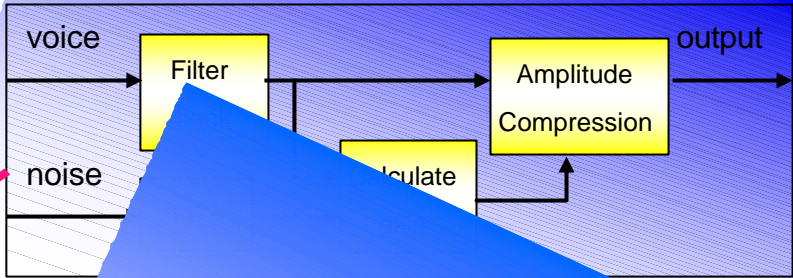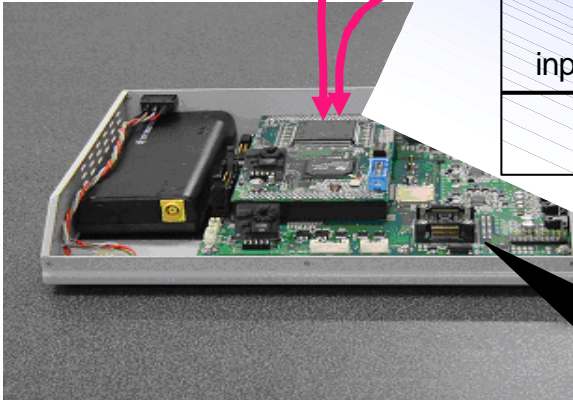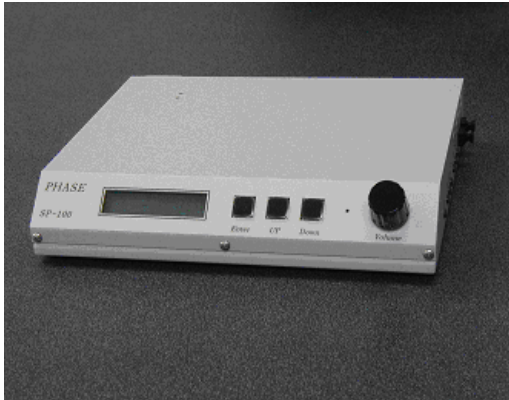
# Fujitsu Network Technologies
## : Verification of media data processing LSI

*Verilog(DUV) model is instantiated in SystemC test bench with SCV*

transaction

signal

SystemC transactor

SystemC module

CPU

CLK1

CPU scenario
1. set register to start DMA
2. detect interruption to finish
3. check status registers
4. check data
5. stop simulation

DUV (HDL)

SC Shell

RAM (A)

CLK1

DMA(1)

RAM (B)

CLK2

DMA(2)

RAM (C)

CLK1

REQ

ACK

random

testbench
（SystemC)
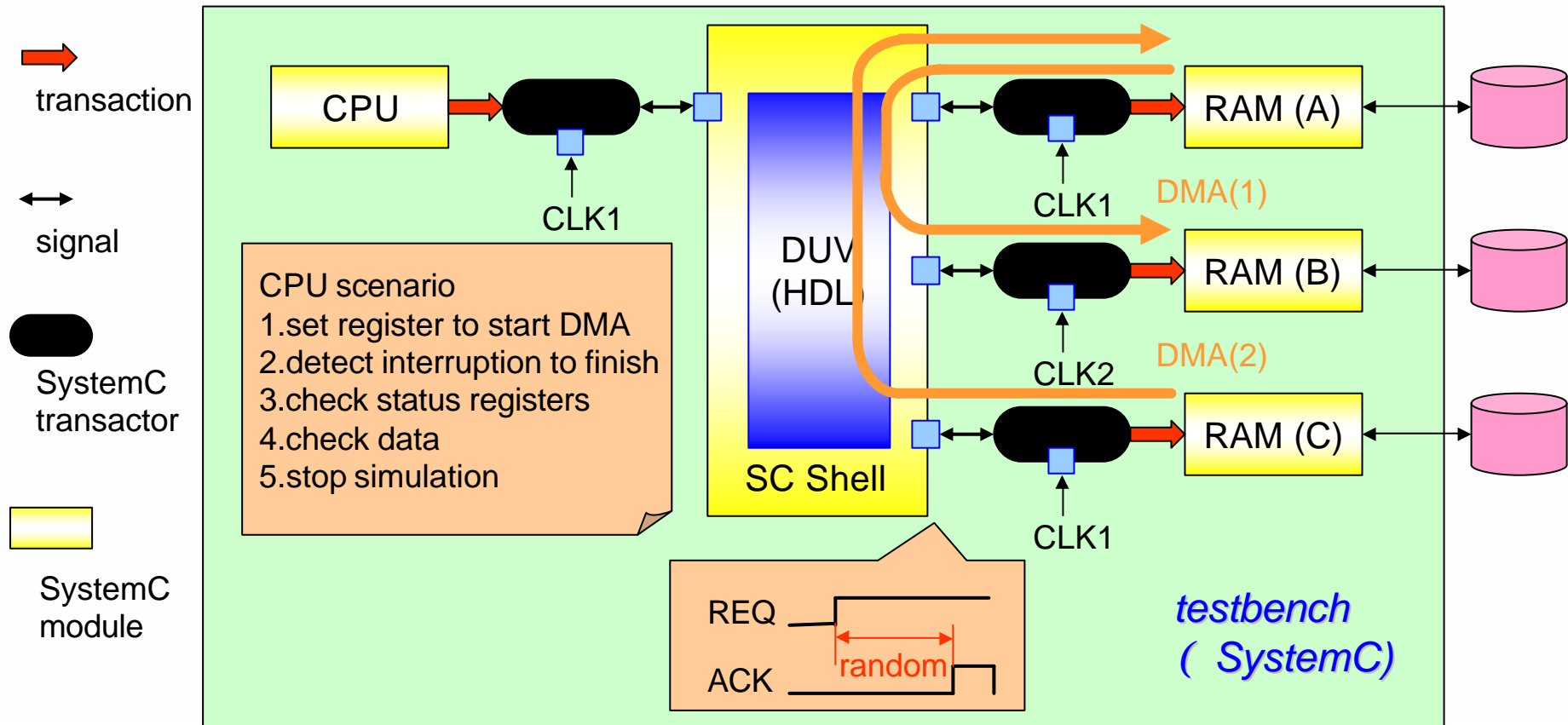
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# NEC Electronics: Design Platform

## ARM®,V850 CPU based design platform in HDL and SystemC



Deliver flexible platform and service to develop the system with re-usable IPs and CPU cores.

Customers can focus on UDL development only.
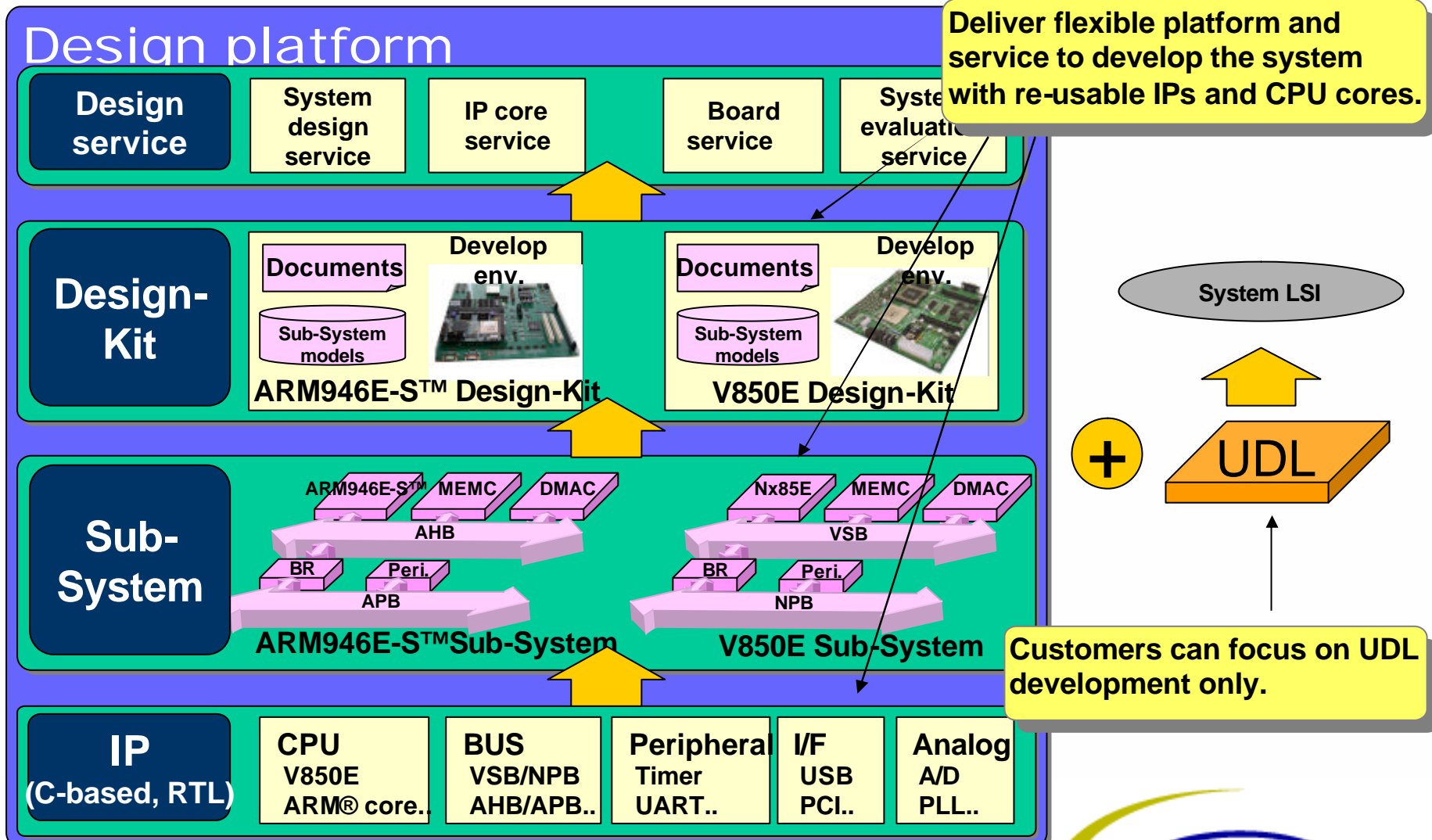
# NEC Electronics: Design flow for platform

- C-based (SystemC) design for new parts
- Synthesize RTL

- Flexible configuration change for bus, memory, IPs, etc,
- Manage the configuration on "Workbench"

**SystemC env.** Debug with GUI

**Behavioral synthesis**

**new design parts (C code)**

C model
RTL

**C-based simulation**

| CPU C model | peri. IP C model | UDL C model |

System bus C model (transaction level)

**IP database (C, RTL, symbol)**

**V850E/ARM® IP**

**CPU core/peri. IP/memory database**

**System configuration**

**System Workbench**

**System LSI**

equivalent

| CPU RTL model | peri. IP RTL model | UDL RTL model |

System bus RTL model (pin/signal level)

**HDL(RTL) env.**

- Varieties of IPs in C and RTL
- Verification model at transaction level
(support AHB CLI by ARM)

- Generate SystemC and HDL environments
- Fast simulation with C-based,
implementation with equivalent RTL

: design and verification environment in design platform

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# Toshiba Media embedded Processor(MeP)

- What is MeP
  - Configurable Processor for Multimedia Application
  - Extensible HW
  - User Custom Instruction and HW accelerator

- Based on SystemC and CoWare environment, we enabled a solution for 'top-down flow' on one MeP: from algorithm to implemented SW and HW accelerator in RTL.
  - MeP Integrator is MeP specific design environment
  - Application is first profiled as SW on the MeP core
  - Then processing intensive function are moved into HW extension
    - User Custom Instruction: UCI, DSP
    - HW accelerator: HWEngine

- By using SystemC TLM Bus models and MeP Module Models in CoWare environment we are enabling solutions for multi-MeP SOC system assembly.

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# Toshiba MeP ConvergenSC Designkit

- **30 days Free Evaluation License Available**
- **CoWare SystemC based ConvergenSC**
- **MeP Integrator**
  - ISS and SW Environment Automatic Generator
  - Extensions with SystemC
    - ◆ UCI and DSP
    - ◆ HWEngine
- **Application**
  - MeP@SoCiation Registration to get User ID and Password
  - URL   http://www.mepcore.com/

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# Summary

- Japanese local seminars, trainings, books, magazines.

- Multimedia is the major application.

- Behavioral synthesis is one of the key technologies.

- SystemC is adopted and utilized by various and major companies in Japan.

**"SystemC in Japan" @11th European SystemC Users Group, 2005**

**SYSTEMC**™