Tools for SystemC Designers
Summit Design, Inc.
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Visual Elite
SystemC graphical capture

Vista
SystemC authoring and debugging

System Architect
SystemC library & related analysis tools
Electronic System Level Design
Products from Summit

Visual Elite
SystemC graphical capture

Vista
SystemC authoring and debugging

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Vista
SystemC Design and Verification

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Smart, Swift, Simple
SystemC user's forum activity

- Compilation/install: 24%
- Code/debug: 43%
- Modeling: 18%
- Compatibility: 0%
- Other: 14%
- Speed: 1%
Vista is an Integrated Development Environment dedicated to SystemC.

Vista supports authoring the code, simulating, debugging and analyzing the design.
Vista architecture

- Vista bundles the standards together…
- Vista’s architecture:
  - OSCI Kernel (2.0.1 & 2.1)
  - GCC Compiler (3.4.3 & 3.3.5)
  - XEmacs Editor
  - GDB Debugger
- Vista leverages on reliable tools:
  - Familiar: quickly up to speed
  - Reliability
Vista supports OSCI and OCP-IP based flows

- **Message Layer (TL3)**
  - Executable Design Spec
  - Functional Architecture Modeling

- **Transaction Layer (TL2)**
  - Executable Architecture spec
  - Physical Architecture Modeling

- **Transfer Layer (TL1)**
  - Executable Implementation spec
  - Module Implementation Specification

- **RTL Layer (TL0)**
  - Implementation
  - Final Implementation

- **Programmer’s View Model (PV)**

- **Programmer’s View + Timing Model (PV+T)**

- **Cycle Callable (CC)**
All C++ member variables are traceable!
- All SystemC/C++ objects can be acquired to the Waveform: int, double, string, enum, struct, ...
- All objects constantly display its value in the browser
Extensions for Vista

- Vista, as an open, non-intrusive, non-instrumented environment supports SystemC extensions:
  - SCV Library (included in Vista release)
  - TLM Library
  - OCP-IP Libraries
  - Any other proprietary or public extension (SimC)

- Summit System Architect
  - …dedicated to architecture analysis
“Summit’s Vista tool was surprisingly easy to adapt into our functional verification flow. It was fully integrated and co-simulating in our environment in less than one day, requiring only minimal changes to our makefiles and environment setup. We are very impressed with Vista’s ease of use and powerful SystemC visualization capabilities. Visualization of SystemC internals has been one of the biggest challenges in our functional verification flow. We believe that Summit Vista improves our verification flow and reduces the total time needed for our verification projects.”

(Harri Syrjä – Bitboys, Verification Manager)
The objective of the 4MORE Project is to complement MATRICE and worldwide research efforts, advancing from implementation through the design of a System on Chip (SoC) for a 4G terminal employing multiple antennas and based MIMO MC-CDMA techniques.

“As a very flexible tool, VISTA has been quickly integrated in our specific design flow. We believe that the powerful debugging capabilities of this product are a big improvement to verify these complex SoCs.”

(Friedbert Berens
– STMicroelectronics Wireless Systems and Algorithms Team Leader)

This project 4MORE (4G MC-CDMA multiple antenna system On chip for Radio Enhancements) is supported by the European IST organization [visit http://ist-4more.org/].

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Thank You

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