6th European SystemC Users Group Meeting

http://www-ti.informatik.uni-tuebingen.de/systemc

Stresa (VB), Italy

October 22nd, 2002, 1100-1700

Thanks

Thank you ST Microelectronics

for sponsoring our

6th European SystemC Users Group Meeting!

Agenda 1100-1300

- **Introduction & Welcome**

  Wolfgang Rosenstiel, University of Tübingen, ESCUG
- **SystemC News**
- **SystemC Business Update**
- **OSCI Working Group Updates**

  Guido Arnout, CoWare, OSCI Chief Strategy Officer
- **SystemC Tools**

  Grant Martin, Cadence
- **SystemC 3.x: SystemC Software Modelling**

  Thorsten Groetker, Synopsys, OSCI Language WG
- **Verification Using SystemC**

  Grant Martin, Cadence
- **Lunch**

Agenda 1400-1500

- **User Presentations – Part 1:**
  - Alberto Sardini, Rational Software, Italy:

    SystemC & UML 2.0
  - Yves Vanderperren, ST Microelectronics, Belgium

    SystemC & UML
  - Francesco Bruschi, Politecnico di Milano, Italy:

    SystemC & UML
  - Rob Slater, Motorola Semiconductors, Israel:

    SystemC Experiences
- **Coffee Break**

Agenda 1615-1715

- **User Presentations – Part 2:**
  - Ilia Oussorov, Infineon Technologies, Germany

    SystemC-Based Gradual Development Flow
  - Francesco Menichelli, University of Rome, Italy :

    A Flexible SystemC Simulator for Microprocessor SoC
  - Nicolas Tribie, CEA/LETI,France:

    A SystemC/HDL Co-Simulation Framework
  - Jens Zellmann, IMMS, Germany:

    Modelling Cycle-Accurate HW with Matlab/Simulink using SystemC
- **Closing**