A Fast and Accurate FPGA-based Fault Injection System

**Problem**

Hardware verification is too slow when using serial fault emulation.

**Proposed solution**

Bypassing the time-consuming synthesis by a direct injection of faults into the FPGA design.

**Static mapping**

Need for a static mapping between FPGA design and circuit description.

**Generation of the static mapping**

Creating a static mapping that provides the fault locations from the circuit description while connecting them to physical primitives on the FPGA.

**Using the static mapping for the fault injection**

Adjusted workflow of the serial fault emulation

**Experimental results**

**Experimental setup**

- Intel Core i5-3470 @ 3.20GHz
- 8GB RAM
- Scientific Linux 6.3 64-bit
- Kernel 2.6.32-279.19.1-2.48.86_64
- Synplify Premier G-2012.09
- Xilinx ISE Tools 14.1i
- Synplify Premier G-2012.09
- Kernel 2.6.32-279.19.1.el6.x86_64
- 8GB RAM

**Circuits under test**

- MIPS32 Processor
  - [ASIC (nangate) | RTL]
  - [ASIC (nangate) | RTL]
- CGRC
  - [ASIC (nangate) | RTL]

**Success rate of the static mapping**

- [Graph showing success rate vs. clock cycles]

**Speedup compared to serial fault emulation**

- [Graph showing speedup compared to serial fault emulation]